
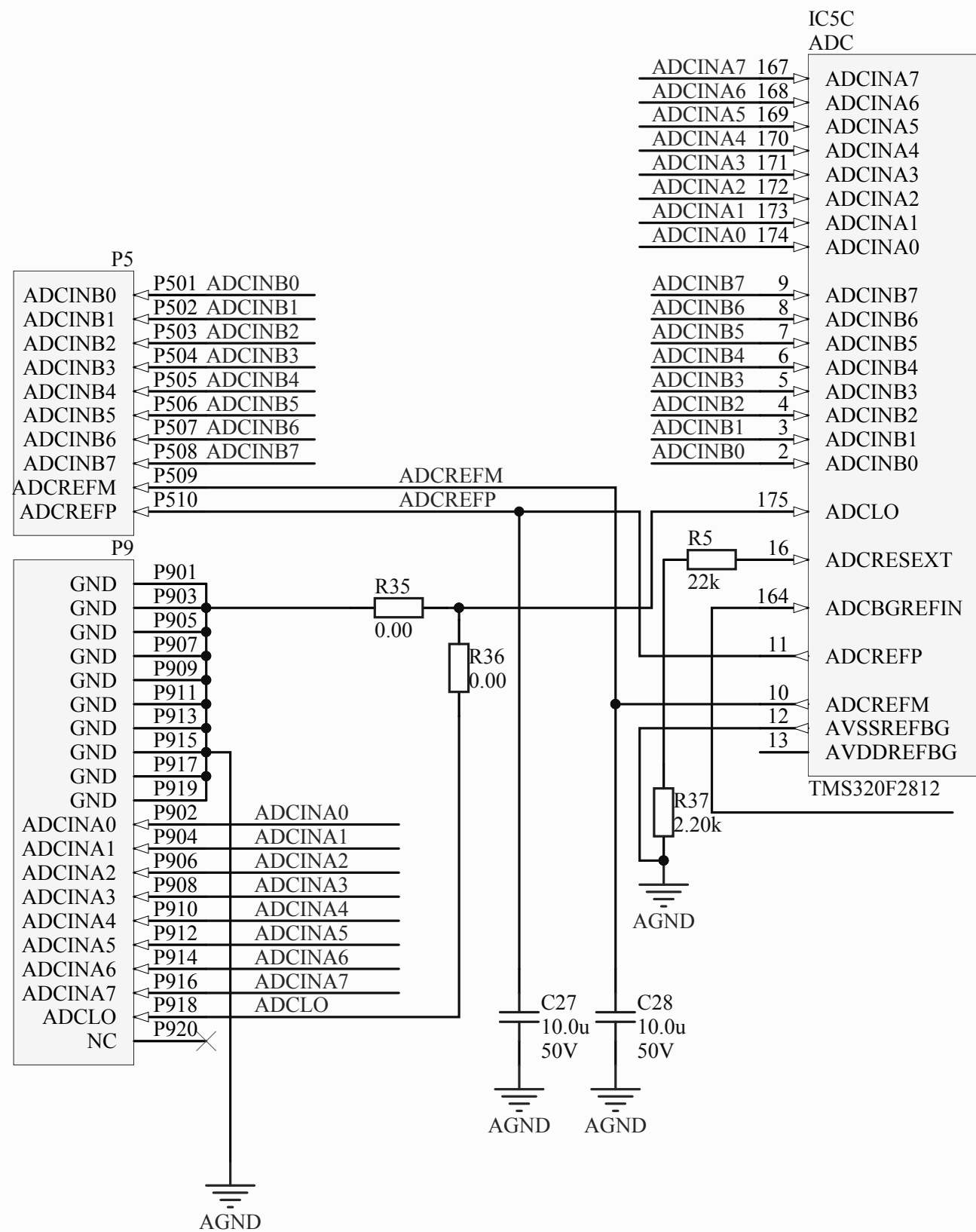
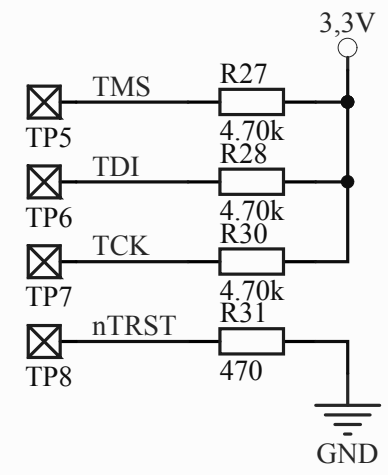
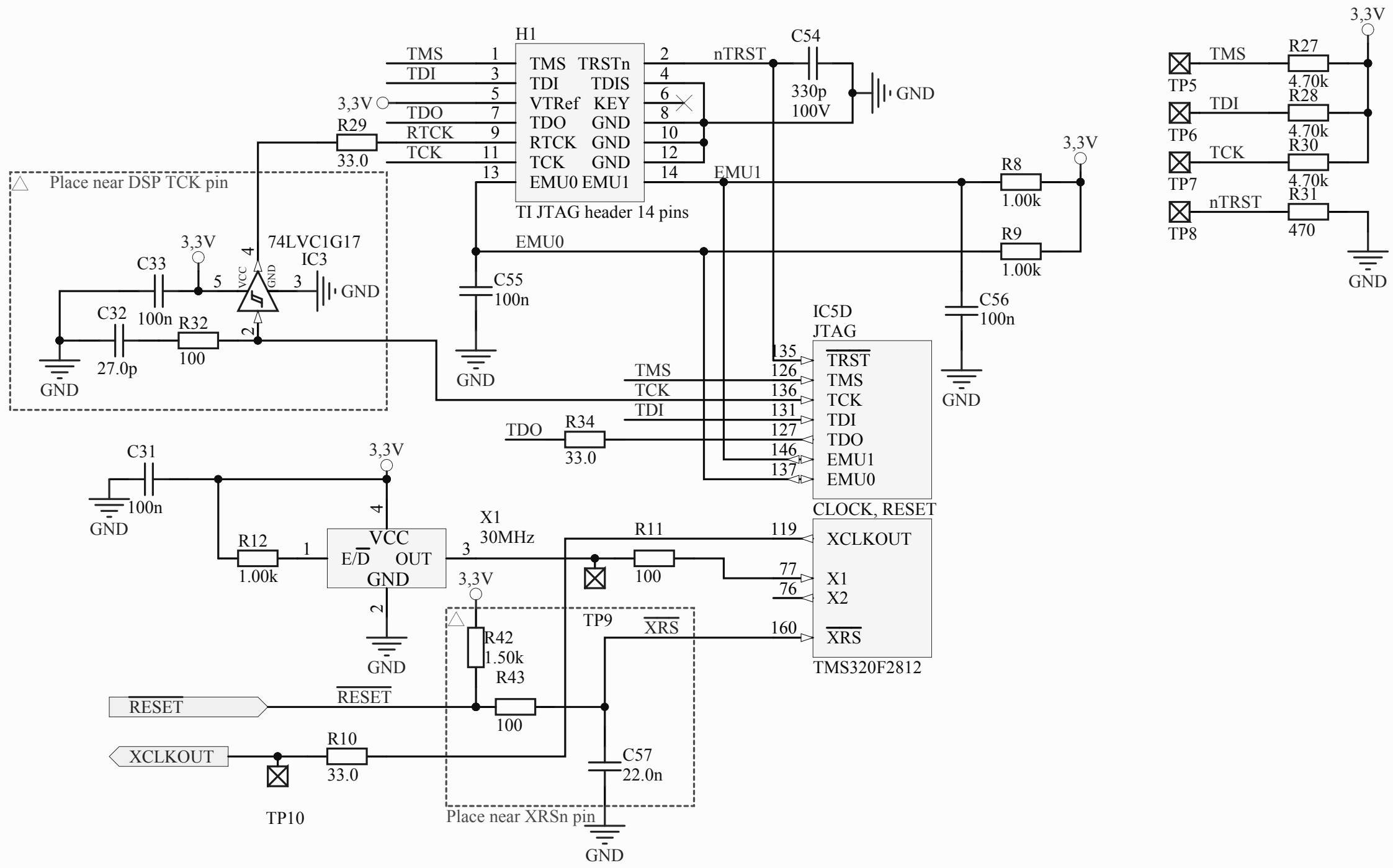
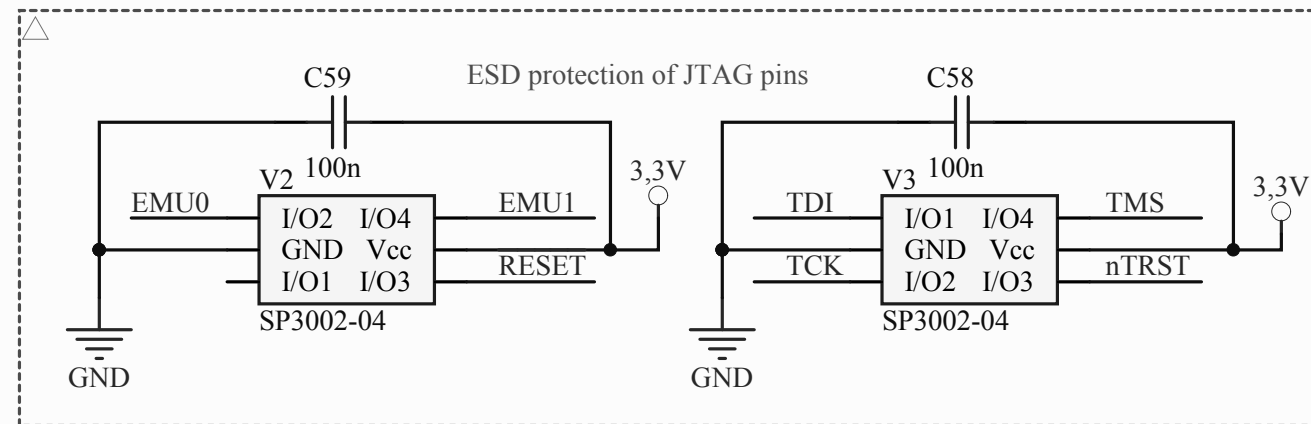


TXA TXA
RXA RXA

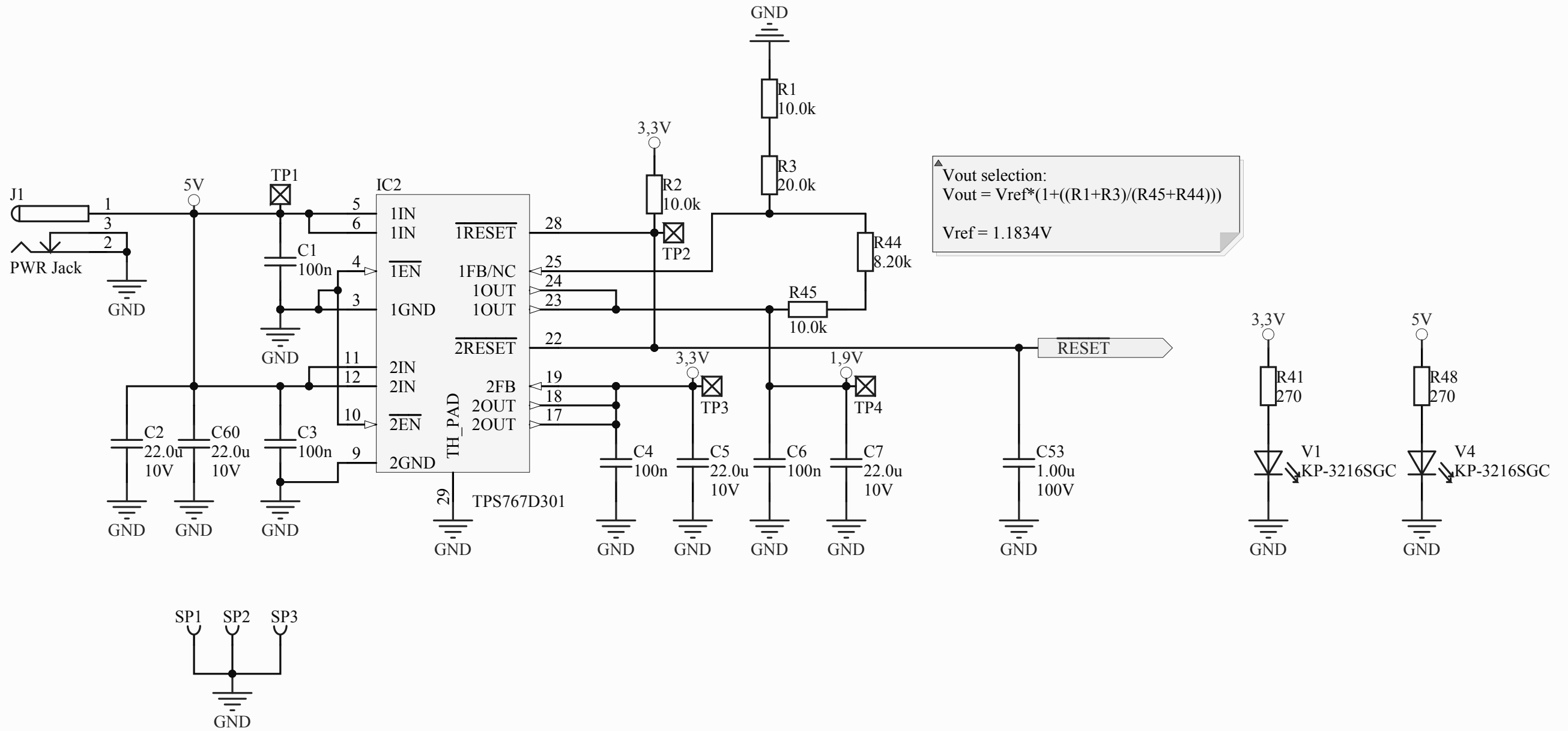
 Regional Innovation Centre for Electrical Engineering Univerzitni 26 306 14 Plzen Czech Republic	Size: A4	Date: 5.8.2014	Title: DSP module for MLC interface	
	Author: Tomas Kosan	Subtitle: [SUBTITLE]		
	Checked by:	Nr.: Sch_Number	Revision: 0.1	
	Approved by:	Type: typ	Sheet 1 of 1	
	File: isoCan.SchDoc			



Size: A4	Date: 5.8.2014	Title: DSP module for MLC interface	
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Checked by:	Nr.: Sch_Number	Revision: 0.1	
Approved by:	Type: typ	Sheet * of *	
	File: Analog_part.SchDoc		



Size: A4	Date: 5.8.2014	Title: DSP module for MLC interface	
Author: Tomas Kosan	Subtitle: Clocking and JTAG connection		
Checked by:	Nr.: Sch_Number	Revision: 0.1	
Approved by:	Type: typ	Sheet * of *	
File: Clock_and_JTAG.SchDoc			

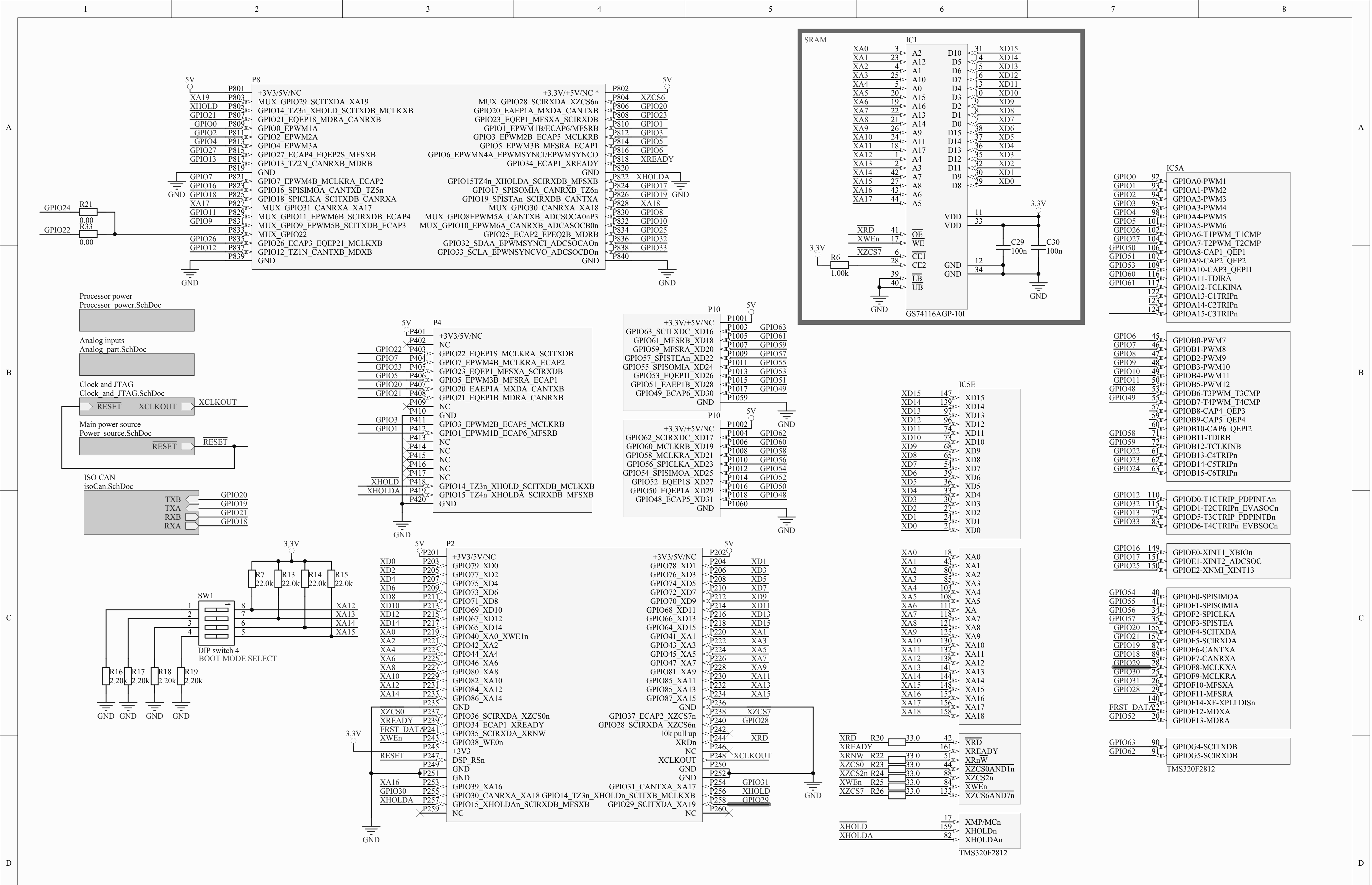


Vout selection:
 $V_{out} = V_{ref} * (1 + ((R1 + R3) / (R45 + R44)))$
 Vref = 1.1834V

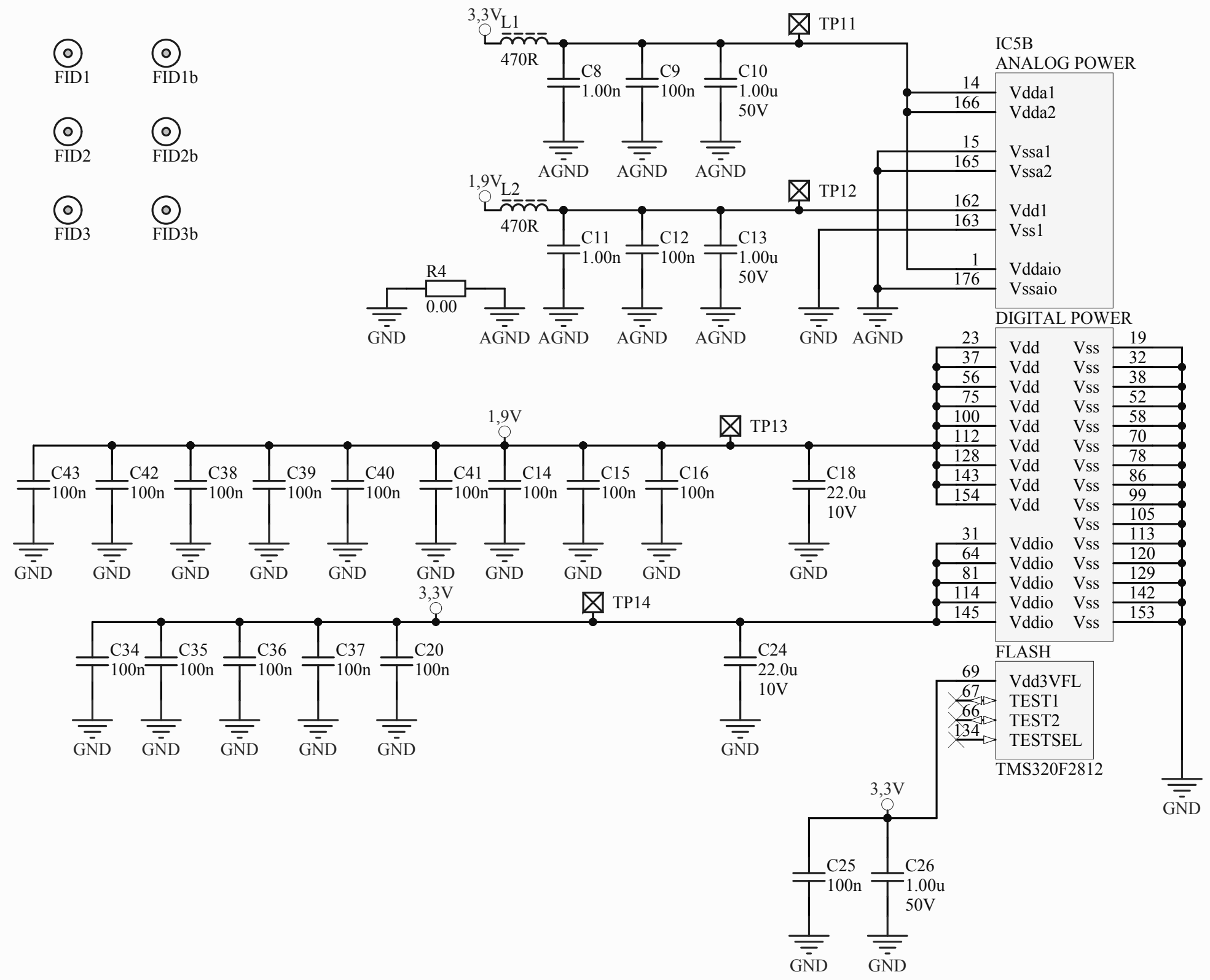


Size: A4	Date: 5.8.2014	Title: DSP module for MLC interface	
Author: Tomas Kosan	Subtitle: Power source 3V3 and 1V9		
Checked by:	Nr.: Sch_Number	Revision: 0.1	
Approved by:	Type: typ	Sheet * of *	
File: Power_source.SchDoc			

Note: Data in fields enter via project/document parameters.



Size: A3	Date: 5.8.2014	Title: DSP module for MLC interface	
Author: Tomas Kosan	Subtitle: Top level schematics		
Checked by:	Nr.: Sch_Number	Revision: 0.1	
Approved by:	Type: Typ	Sheet * of *	
File: processor.SchDoc		Note: Data in fields enter via project/document parameters.	



Size: A4	Date: 5.8.2014	Title: DSP module for MLC interface	
Author: Tomas Kosan	Subtitle: [SUBTITLE]		
Checked by:	Nr.: Sch_Number	Revision: 0.1	
Approved by:	Type: typ	Sheet * of *	
File: Processor_power.SchDoc			